



UNITED STATES PATENT AND TRADEMARK OFFICE

14A

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|-----------------------------|-------------|----------------------|---------------------|------------------|
| 10/713,198 | 11/17/2003 | Seung Hee Nam | 8733.936.00-US | 9565 |
| 30827 | 7590 | 06/23/2006 | EXAMINER | |
| MCKENNA LONG & ALDRIDGE LLP | | | QI, ZHI QIANG | |
| 1900 K STREET, NW | | | ART UNIT | |
| WASHINGTON, DC 20006 | | | PAPER NUMBER | |
| | | | 2871 | |

DATE MAILED: 06/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| | | | |
|------------------------------|--------------------------------------|-----------------------------------|--|
| Office Action Summary | Application No. 10/713,198 | Applicant(s) NAM ET AL. | |
| | Examiner Mike Qi | Art Unit 2871 | |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 27 April 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-6 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-6 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on April 27, 2006 has been entered.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1, 2 and 4-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6,380,559 B1 (Park et al).

Regarding claim 1, Park discloses (col.6, line 51 – col.13, line 52; Figs.1-5) that a fabrication method of a liquid crystal display panel comprising:

- forming a thin film transistor (3) at crossings of gate lines (22) and data lines (62) formed on a substrate (10); and the forming process by using mask (see col.2, lines 55-59) that would be in a first masking process;
- providing a substrate including a plurality of thin film transistor array substrates, such as four panel regions (110,120,130,140) corresponding to

four display areas (111,121,131,141) (four thin film transistor array substrates) having a gate line assembly (gate pad part formed thereon) including a gate pad (24) connected to the gate line (22) and a data line assembly (data pad part) including a data pad (64) connected to the data line (62); and the data line assembly (data pad part) including lower layer (621, 641, metallic material) and upper layer (622, 642, low resistance metallic material), that is the data pad and data pad protection electrode functions to protect the data pad; and those process by using mask (see col.2, lines 59-64) that would be in a second masking process;

- forming passivation layer covers the data line assembly (including data pad) i.e., data pad protection, and forming pixel electrode by using mask (see col.2, line 65 – col.3, line 18) that would be in a third masking process.

Although Park does not explicitly disclose arranging a cutting-off plate on a remainder region of the substrate other than the region of the pad (display area), and exposing the gate pad of the pad part and the data pad protection electrode (peripheral area) by an etching process using the cutting-off plate, Park teaches (col.10, line 26 – col.12, line 67; Figs.9-12) that the etching process using mask (such as mask 300 and 400).

The function of the cutting-off plate is the same as the function of a mask, because the cutting-off plate having open portion and opaque portion that allows the light passing through the open portion; and using mask to expose the gate pad of the pad part and the data pad electrode by etching process using a mask, and arranging a

Art Unit: 2871

mask on a region to form the pad part, so that the opaque portion on a region of the substrate other than the region of the pad part. Park indicates (col.10, lines 28-45) that the light exposure at the display area D is different from the light exposure at the peripheral area P, such that the molecules at the display area and at the peripheral area being resolved by using mask to a predetermined depth from the surface.

Therefore, it would have been obvious to those skilled in the art at the time the invention was made to modify the fabrication method of a liquid crystal display panel of Park with the teachings of arranging a mask (cutting-off plate) and exposing the gate pas and the data pad protection electrode by etching process using the mask (cutting-off plate) as taught by Park, since the skilled in the art would be motivated for obtaining the molecules at the display area and at the peripheral area being resolved by using mask to a predetermined depth from the surface (col.10, lines 28-45).

Regarding claim 2, Park discloses (col.1, lines 13-24) that generally, liquid crystal display is formed with two glass substrates (TFT array substrate and color filter substrate), and the forming method performing photolithography by using mask. Such that the gate pad and the data pad electrode are exposed, and that is a general manufacturing method, and that would have been at least obvious.

Regarding claim 4, Park discloses (col.6, line 51 – col.13, line 52; Figs.1-5) that a fabrication method of a liquid crystal display panel comprising:

- forming gate line assembly (gate pattern) including gate electrode, gate line, gate pad by using mask (see col.2, lines 55-64) that would be by use of a masking process;

Art Unit: 2871

- forming a gate insulation film (30) on the substrate (10) where the gate pattern is formed;
- forming data line assembly including source electrode (65), drain electrode (66), data line (62), data pad (64), storage capacitors (such as pixel electrode 82 overlapped with gate line 22), and semiconductor pattern is formed by etching the passivation layer (see col.2, line 59 – col.3, line13); and such forming process by using second mask, that would be by use of a second masking process;
- forming pixel electrode by using mask (see col.3, lines 14-17), and the pixel electrode (82) is connected to the drain electrode (66), and the pixel electrode can be a storage electrode, and such transparent electrode (pixel electrode) pattern including a data pad protection electrode (such as double layered structure 642, 641 for the data pad 64), and such process is formed by mask, and that is by a third masking process.

Regarding claims 5 and 6, Park teaches (col.3, lines 29-30) that the etching for forming the gate pad and data pad being performed by using dry etching.

3. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over US 6,380,559 B1 (Park et al) as applied to claims 1, 2 and 4-6 above, and further in view of US 6,255,130 B1 (Kim).

Regarding claim 3, Park teaches the invention set forth above except for that the cutting-off plate is made of a metal.

Kim discloses (col.9, lines 49-63; Fig.7B) that a photomask (400) having a plurality of slits (410) (open portion), and a metal Cr layer is coated on the mask (400) to reduce the amount of exposing light.

Therefore, it would have been obvious to those skilled in the art at the time the invention was made to modify the fabrication method of a liquid crystal display panel of Park with the teachings of using a metal cutting-off plate as taught by Kim, since the skilled in the art would be motivated for achieving efficiently shield the light exposing in the opaque portion of the cutting-off plate (col.9, lines 60-64).

Response to Arguments

4. Applicant's arguments with respect to claims 1-6 have been considered but are moot in view of the new ground(s) of rejection. According to the reconsideration of the claims written, the reference such as park can read the limitations as claimed as set forth above, and that would have been at least obvious. The forming process as claimed in which the forming process comprising a masking process (a first masking process), a second masking process and a third masking process that does not definitely define the process only using three masking process.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mike Qi whose telephone number is (571) 272-2299. The examiner can normally be reached on M-T 8:00 am-5:00 pm.

Art Unit: 2871

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



Mike Qi
Patent examiner
June 13, 2006